Dynamically Reconfigurable Logic and System on Chip

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Dynamically Reconfigurable Logic

- Dynamic reconfiguration is a property of a set of logic/computing resources
  - Any set must be well-defined

- FPGAs are classified as dynamically reconfigurable iff ...

  their embedded configuration storage circuitry and corresponding circuit functions can be updated selectively without disturbing the operation of the remaining device logic

- These devices can thus be selectively reconfigured while still active

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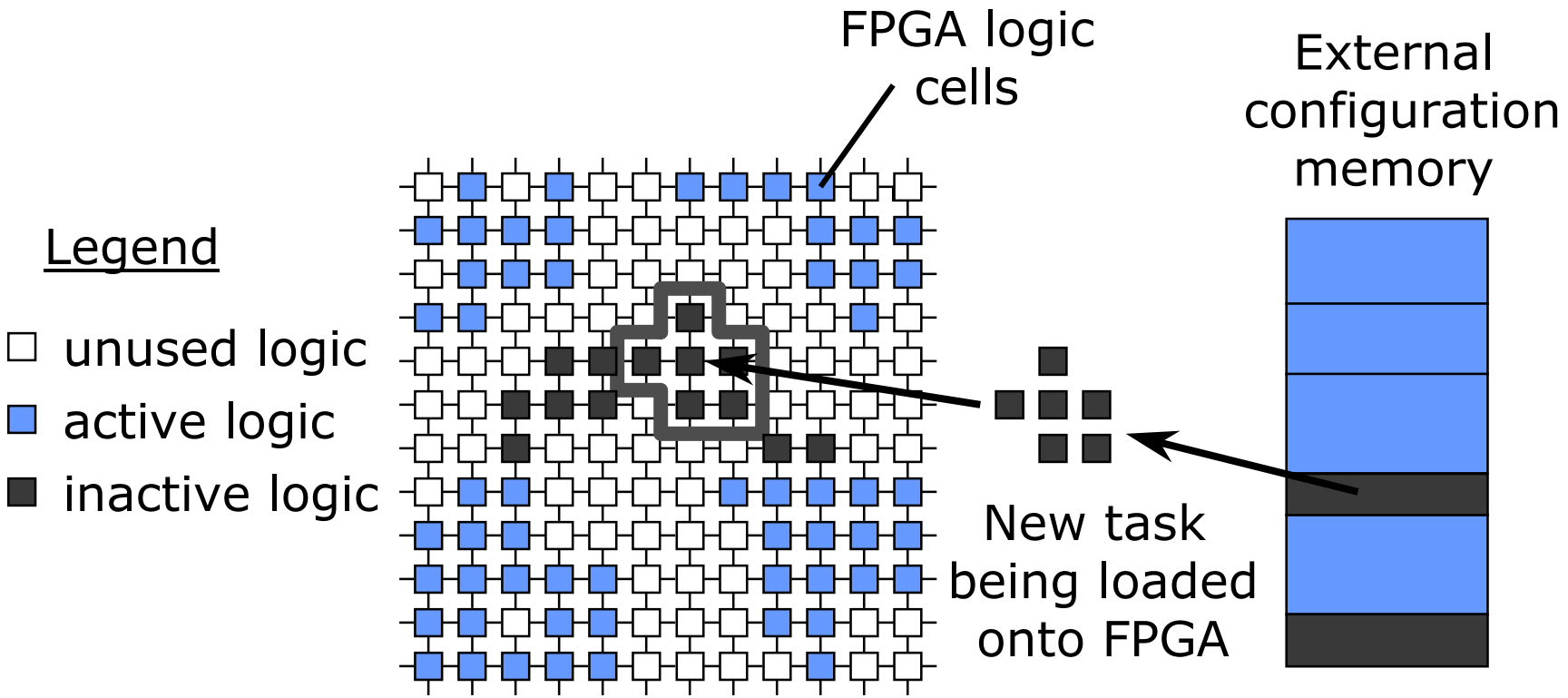
Logic Caching



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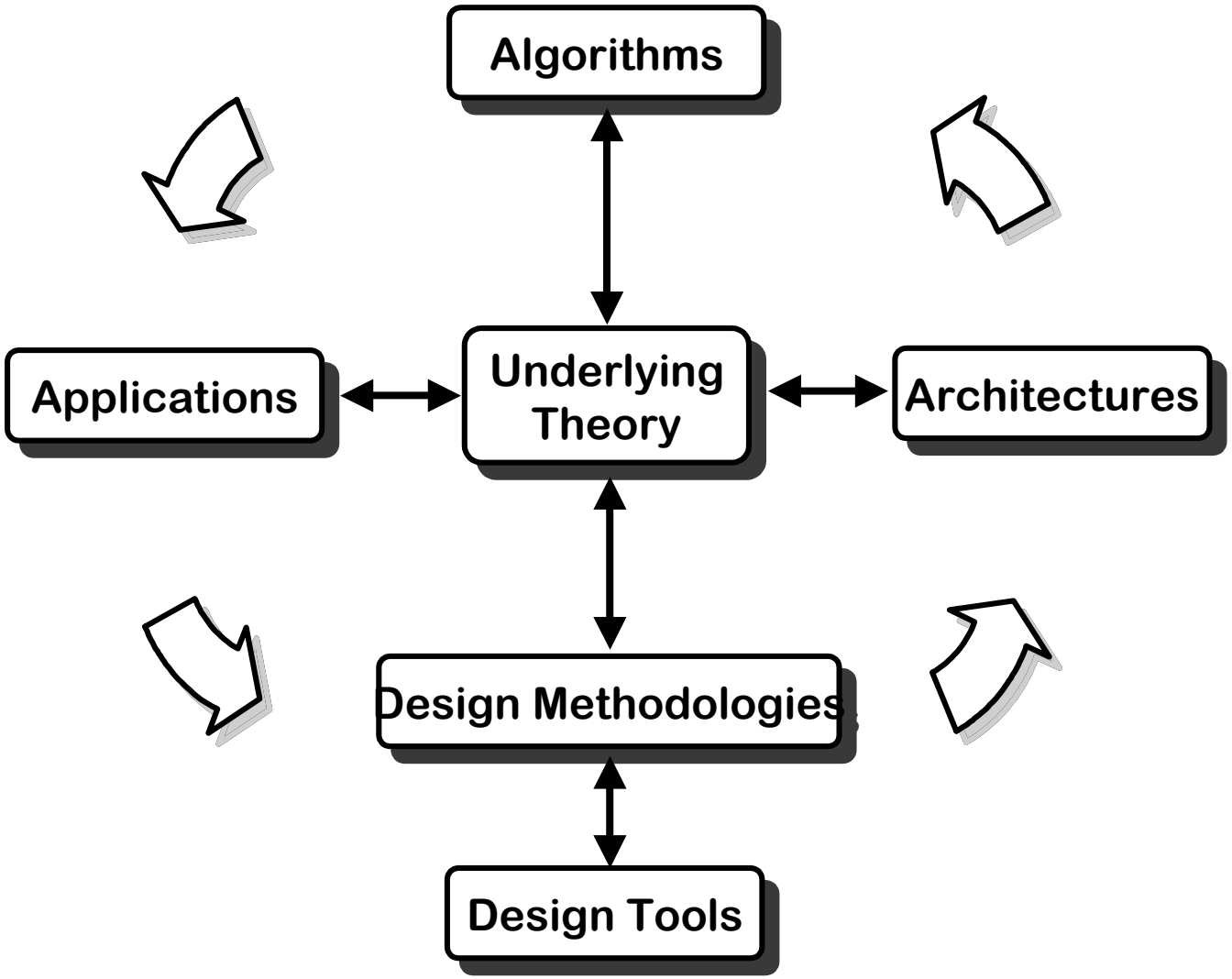
DRL: the research challenge



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DRL

- For conventional designs, there is a one-to-one mapping between logic circuits and physical device resources
- For reconfigurable designs, there is a many-to-one mapping between logic circuits and certain subsets of the physical device resources
- The floorplan is a function of time
- We need CAD tools to design such systems but most CAD vendors refuse to offer tools that are sufficiently customisable
- The pushbutton, black-box approach still has too many advocates

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Dynamic Circuit Switching (DCS) design tools for DRL

- We must re-use human IP by evolving current design knowledge and practices where feasible
  - There is a mental bottleneck
- Capture design intent (VHDL & RIF)
- Simulate dynamic reconfiguration
- Synthesise reconfiguration controller
- Technology map and back-annotate dynamically reconfigurable design (SDF)
- Support circuit verification with monitors and coverage tools

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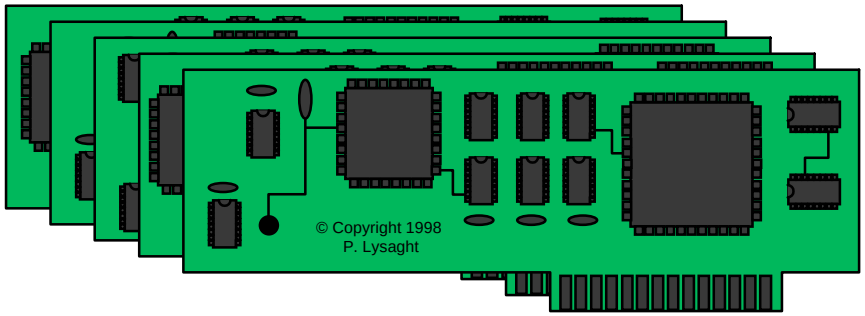
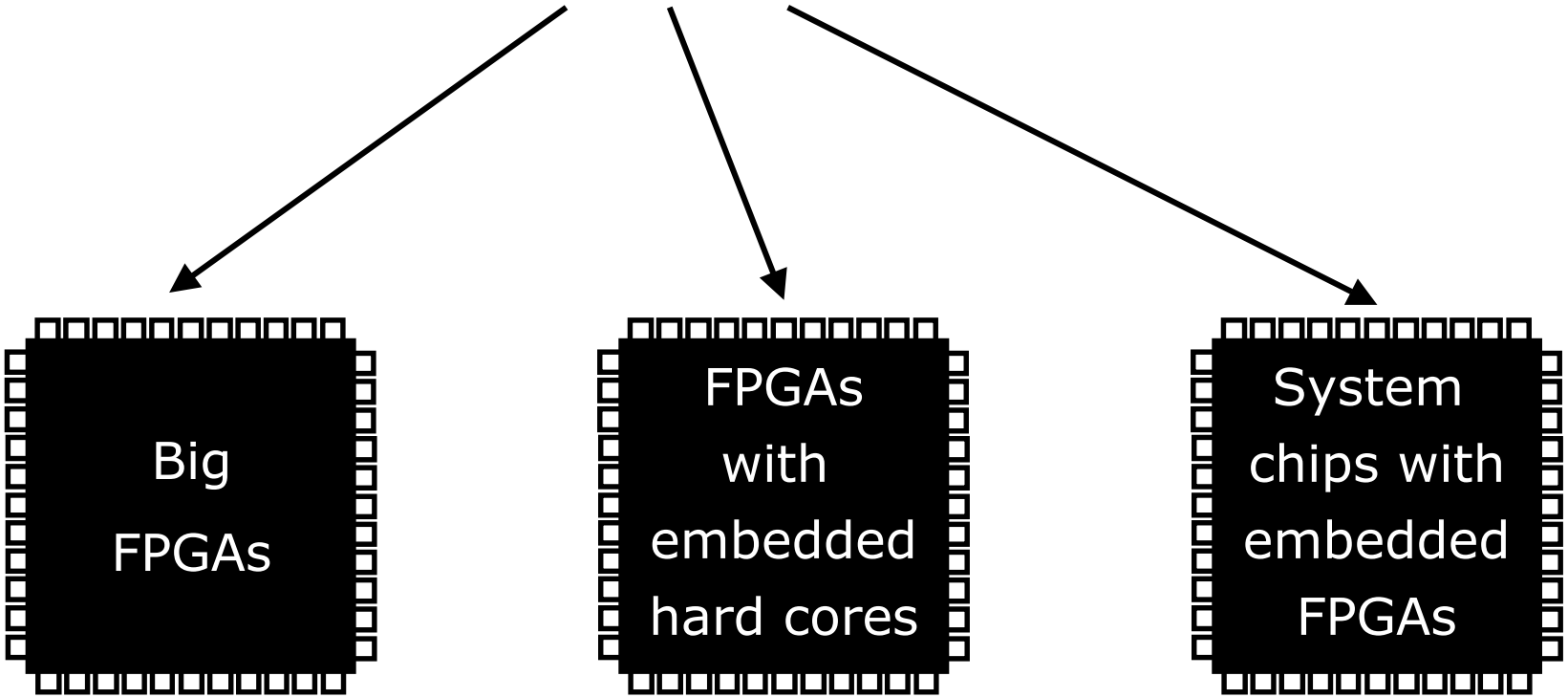
SoC and FPGAs: SoRC/SoPC/CSoC





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SoC and DRL

- SoC makes DRL more viable … counter-intuitive!
  - With more logic and more tasks on a single FPGA, it is significantly less likely that all tasks will execute simultaneously
  - The additional logic needed to reconfigure large circuit blocks is amortised more easily
  - Large FPGAs are expensive even in high volume
  - The difference in the number of gates between adjacent members of a single device family is increasing

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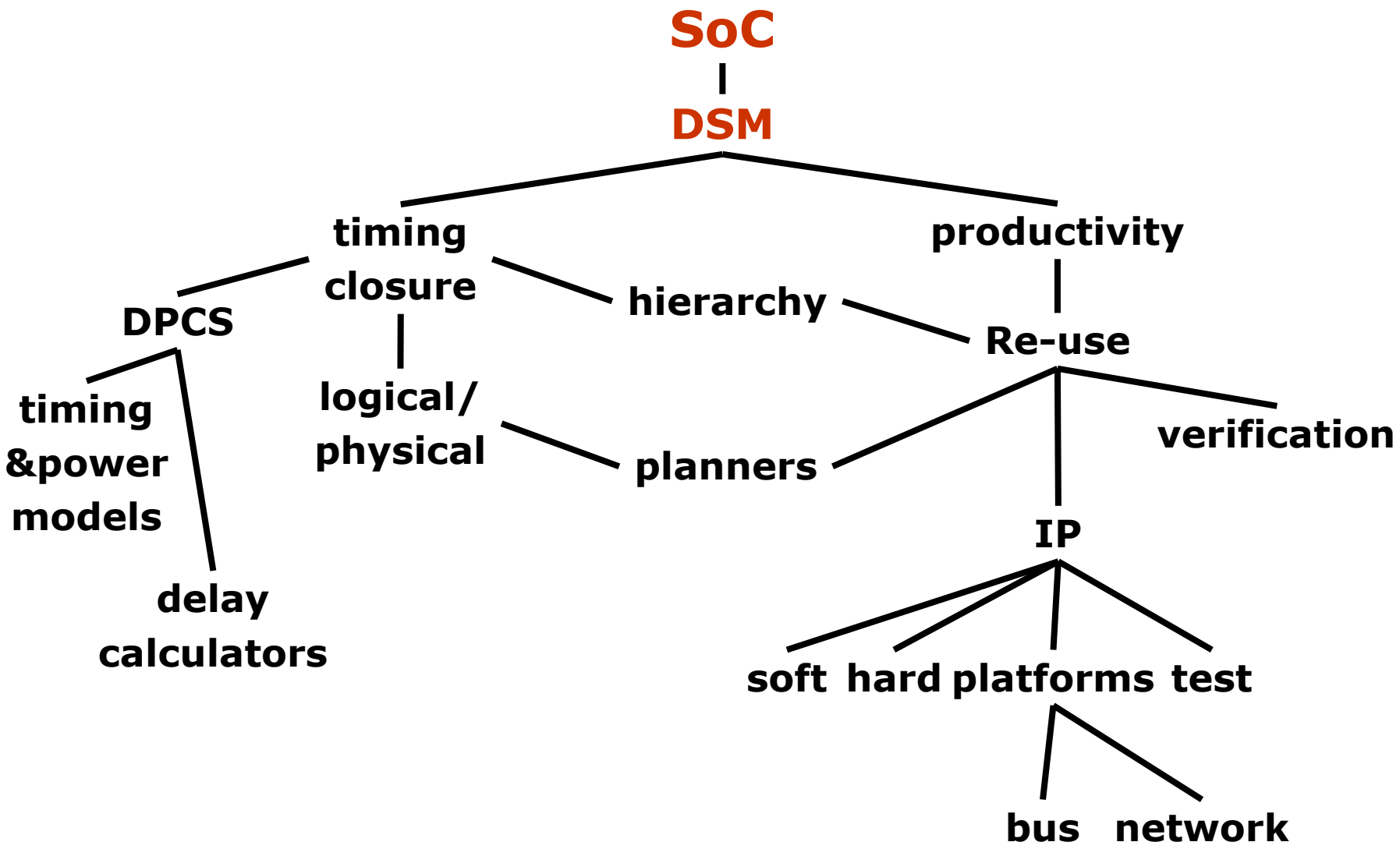

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DSM and SoC design flows

- SoC is synonymous with deep sub-micron (DSM) ASIC technology (< 0.5 micron)
- Moore's Law = more and more, smaller transistors
  - The DSM design flow
    - the smaller size of the transistors and the increasing influence of routing
  - The SoC design flow
    - the productivity challenges of designing with so many transistors (500k transistors +)
- The SoC flow is built on top of DSM flow and is a "block-based" design methodology

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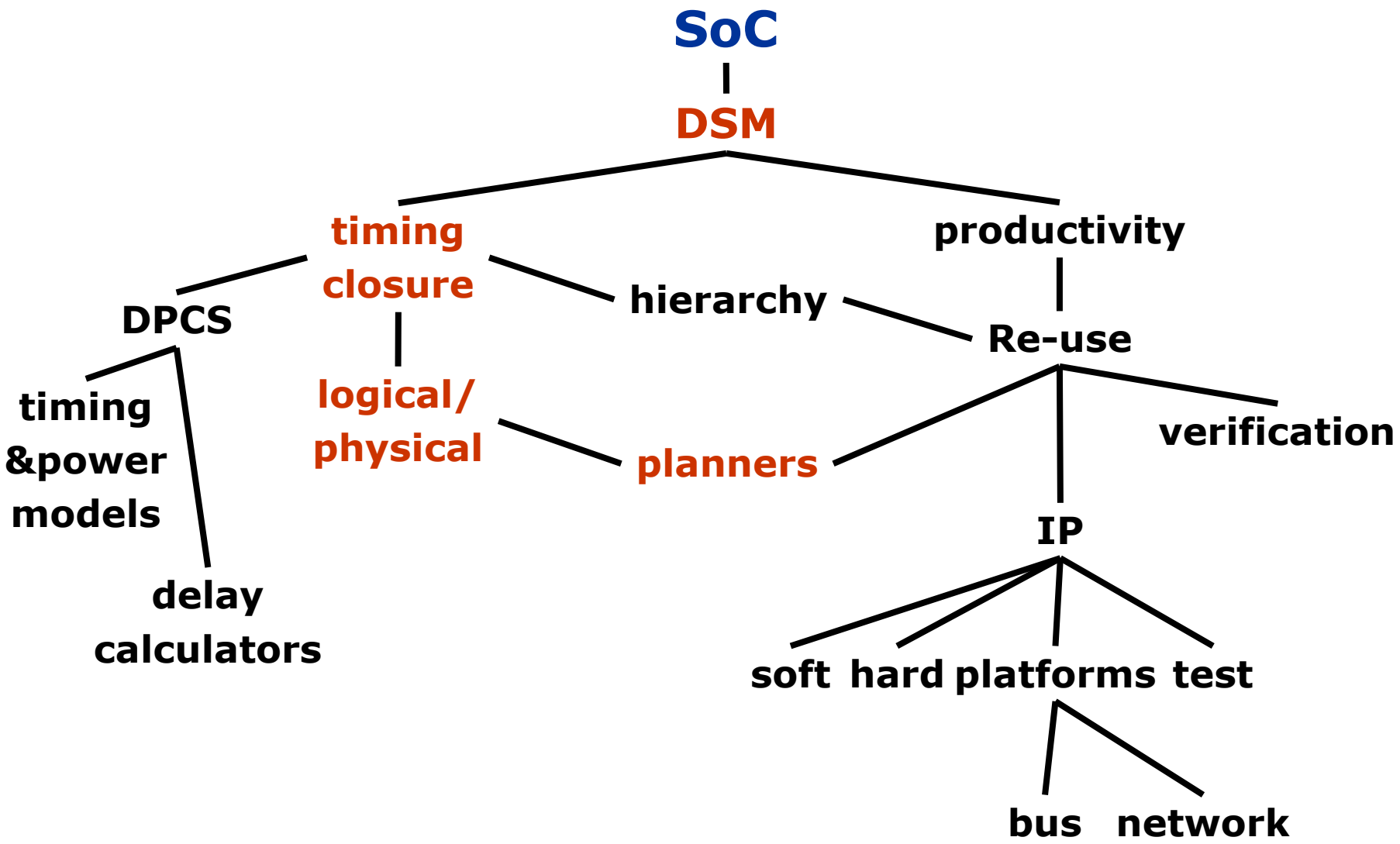

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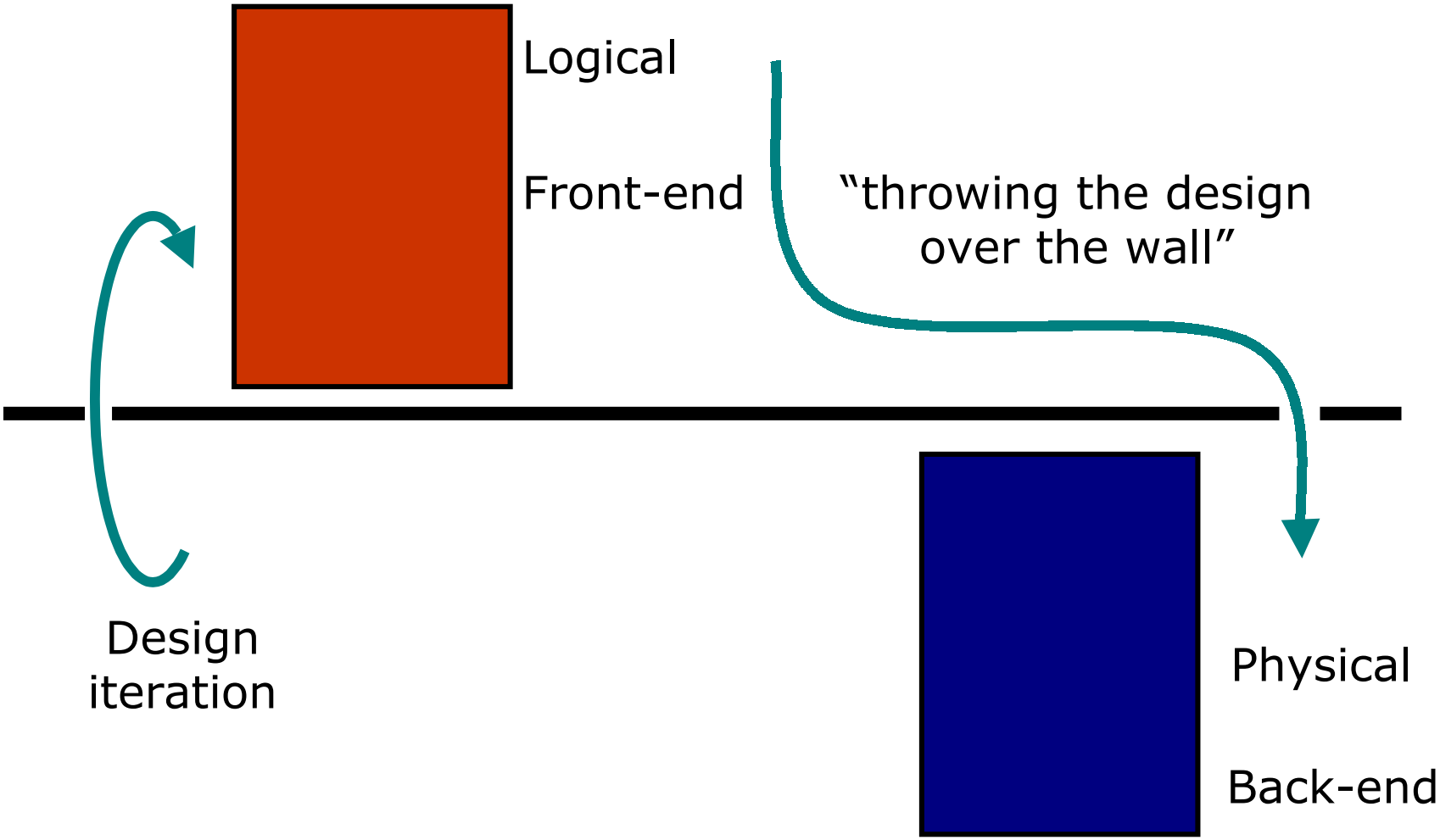
Traditional ASIC design flow



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Solution

- DSM needs better timing (& power) information
- Solving the problem
  - Introduce floorplanning alongside synthesis
  - Estimate timing after floorplanning, placement and global routing
  - Use custom wire-load models
  - Improve timing information models and delay calculation engines
- Also, use newer synthesis tools with constraints for low power design

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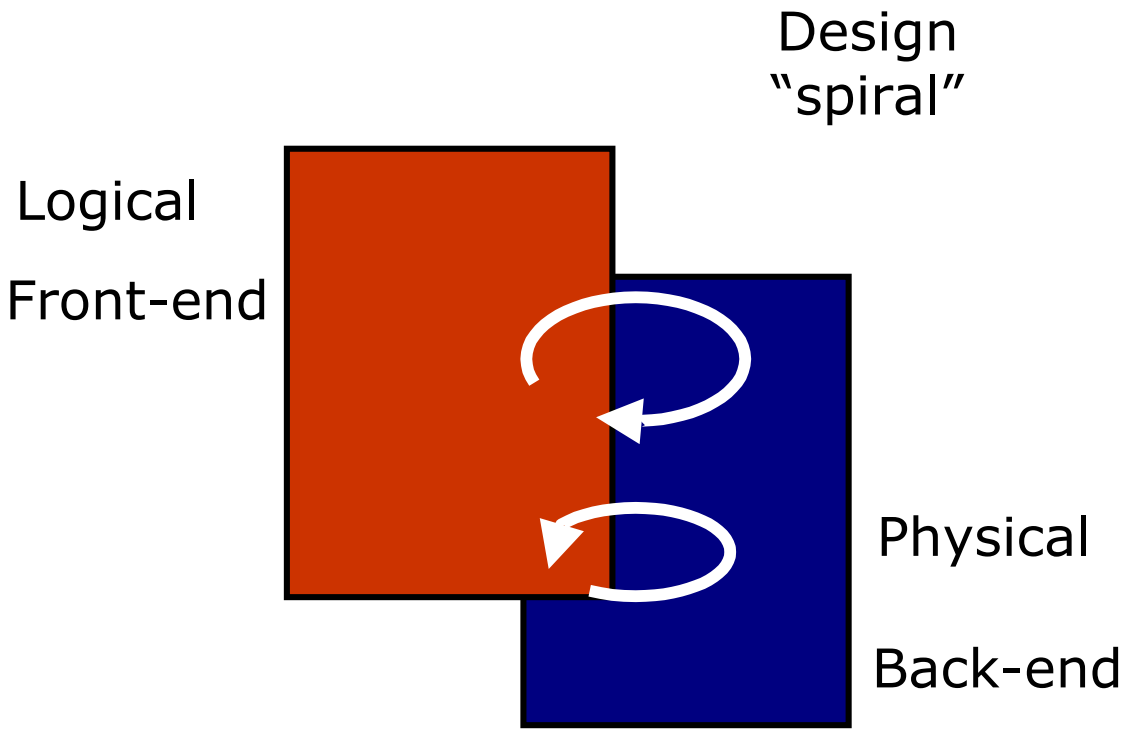
DSM design process



Characterised as: integrated, incremental and iterative

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DSM flow is good for DRL!

- Consider reconfiguration latency estimation
- We need to be able to floorplan the design
  - A global route would be helpful
- This gives us the ability to estimate reconfiguration bitstream size and hence reconfiguration time
- These early, accurate estimates of system reconfiguration latencies allow us to better explore the design space before doing detailed physical design
- Effectively, “custom latency models” versus “statistical latency models

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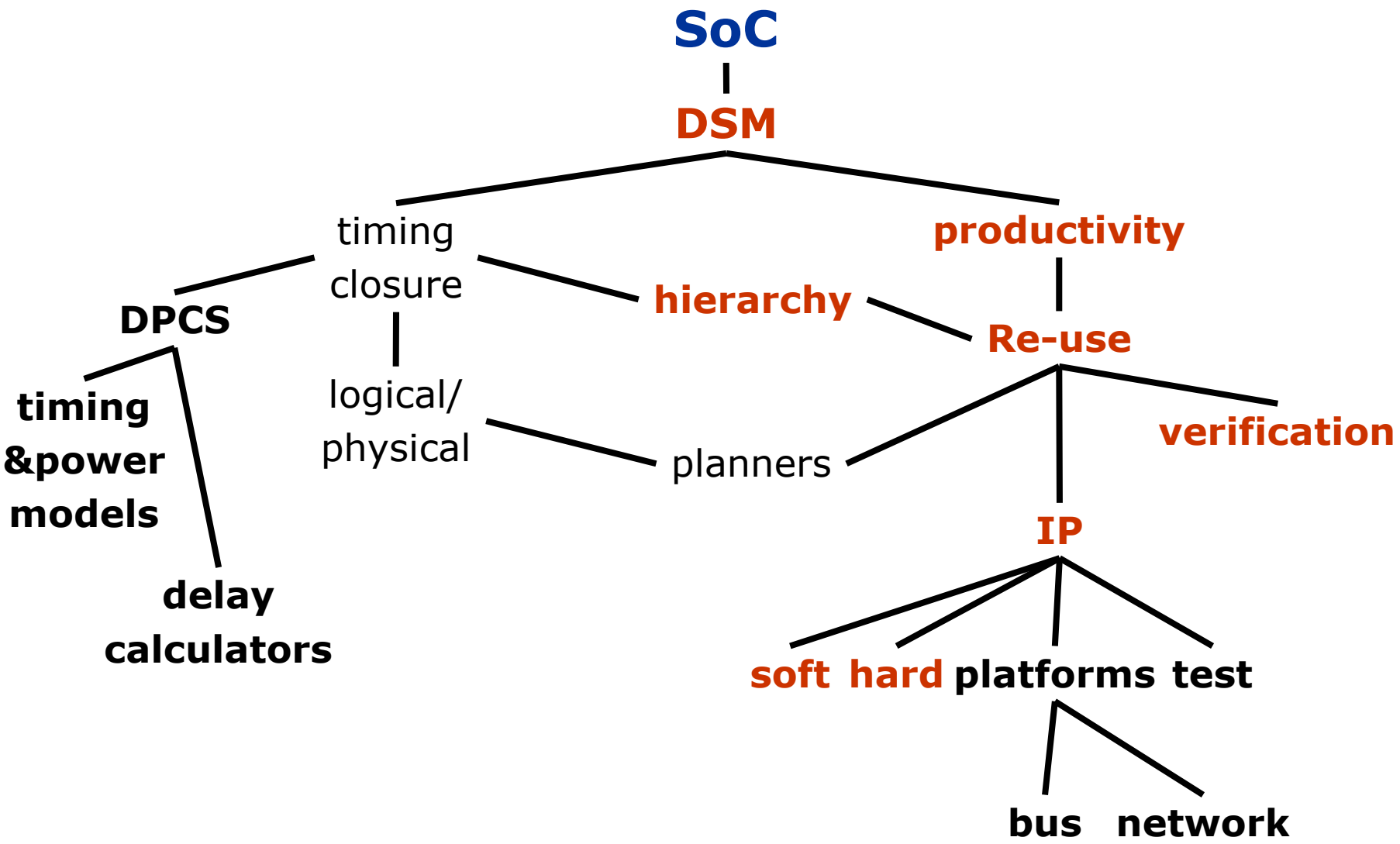

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Design re-use on unprecedented scale

- What is being proposed for SoC is
  - A major increase (90+%) in the amount of design re-use
  - A major increase in the number and range of re-usable components
  - Re-use within and among companies
  - Elevation of re-use to the level of strategic corporate objective
  - Global, net-based market-place for re-usable components
  - Whole new industry with new business models
- This has never been done before in an ASIC design flow

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Soft & hard IP

- Soft
  - Synthesisable RTL code
  - No foundry, process or device dependence
  - Very portable
  - Easily modified
  - Difficult to protect
  - Performance unknown
  - Lowest value
- Hard
  - GDS II (polygon) form
  - Process specific
  - Performance data is available
  - Not portable
  - Easiest to protect via watermarking
  - Difficult to modify
  - Very high value for complex cores

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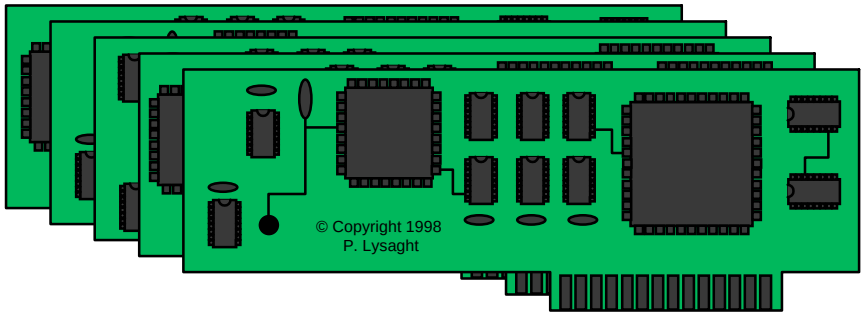
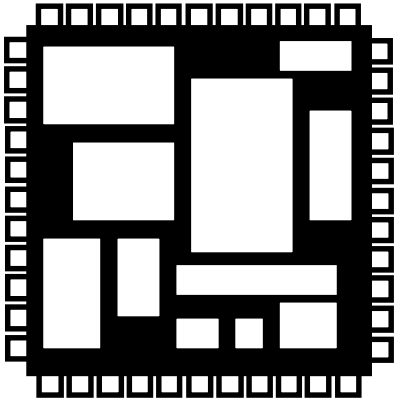
SoC and design re-use

Early 1990's



Late 1990's



System complexity in silicon is
now so great that it necessitates
large-scale design re-use for the first time

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Fast product turnaround assumes pre-verification

- Derivative design cycle: second or third product "spin" of original product
- Derivative product is is differentiated by some critical alterations
  - Customisation for local markets, moving features from software to hardware …
- Verification dominates the design process
- "Pre-staged" design blocks are fully verified
  - Help to hierarchically partition verification
- SoC will be heavily dependent on fully verified blocks

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Block-based design methodologies are good for DRL

- Older physical design tools flattened everything
  - Design hierarchy was lost - all hierarchical, structural information was discarded
- A case of … “the CAD company knows best”
- But re-use demands tools that preserve hierarchy
- Excellent news for DRL, but when will the FPGA tools adopt this approach?
  - Very soon, as SoC becomes important for FPGAs

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New IP options 1: application-specific FPGAs

- Soft FPGA IP block
- Configurable at compile time
- Portable across processes
- Consider CPU cores
  - Like the Tensilica or ARC soft IP ...
  - Reconfigurable application-specific instruction sets with customised software tools
- Now try it with FPGAs
  - Application-specific logic, routing, memory and I/O with customised software tools

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New IP options 2: Dynamically reconfigurable IP

- Dynamically reconfigurable IP (DRIP) blocks
- Configurable at run time
- Consider a UART with many operating modes
  - One mode is used at a time and reconfiguration is infrequent and user-driven
- Explore the trade-offs in configuring only one instance of it at any time on the FPGA and dynamically reconfiguring it in response to user requests
- What would DRIP look like?
  - What are the deliverables?

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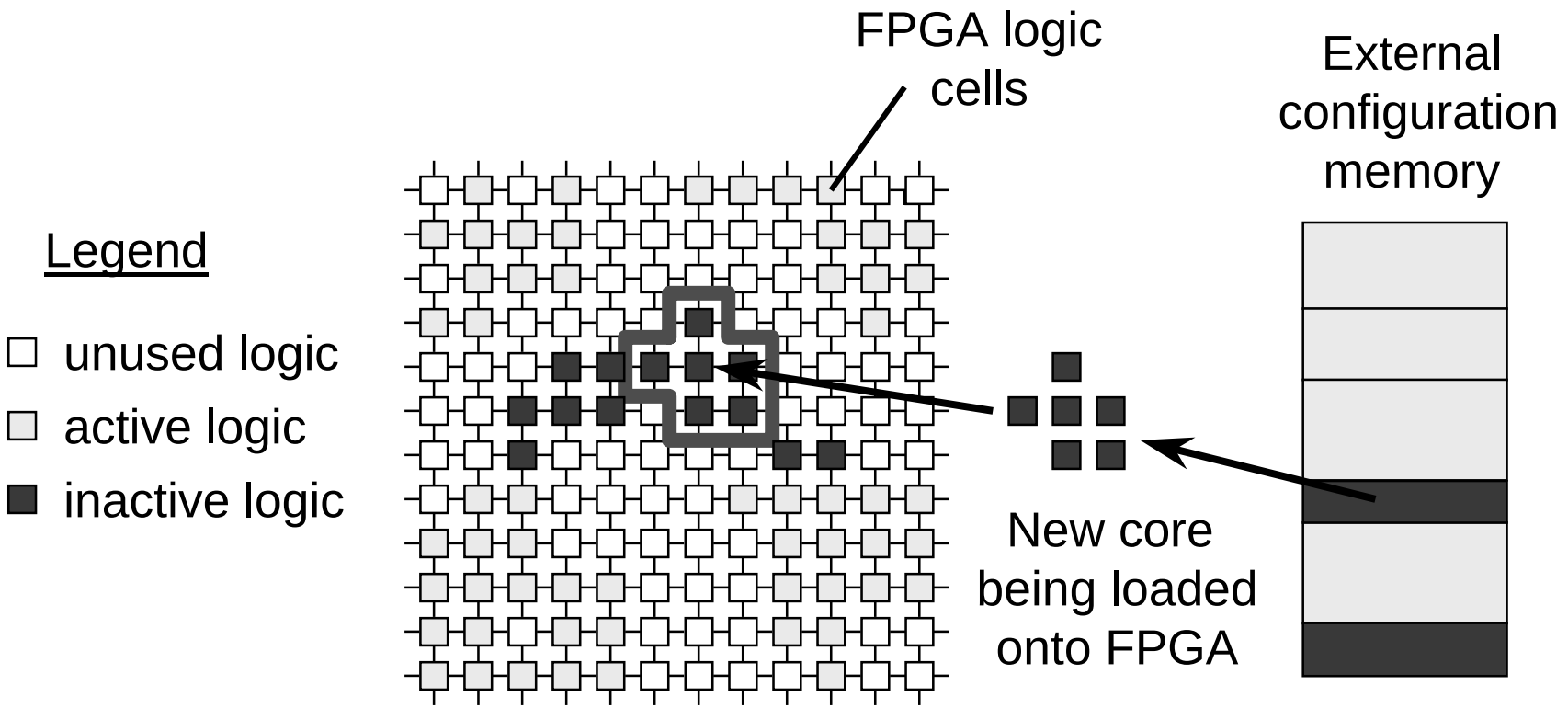
Logic Caching ...
dynamically reconfigurable IP cores



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Free IP

- Collectively we need access to IP
- Cannot afford IP
- Roll your own?
- Must be collaborative?
- We need free IP in the same way that we GNU and LINUX
- We need an open, synthesisable FPGA with associated tools

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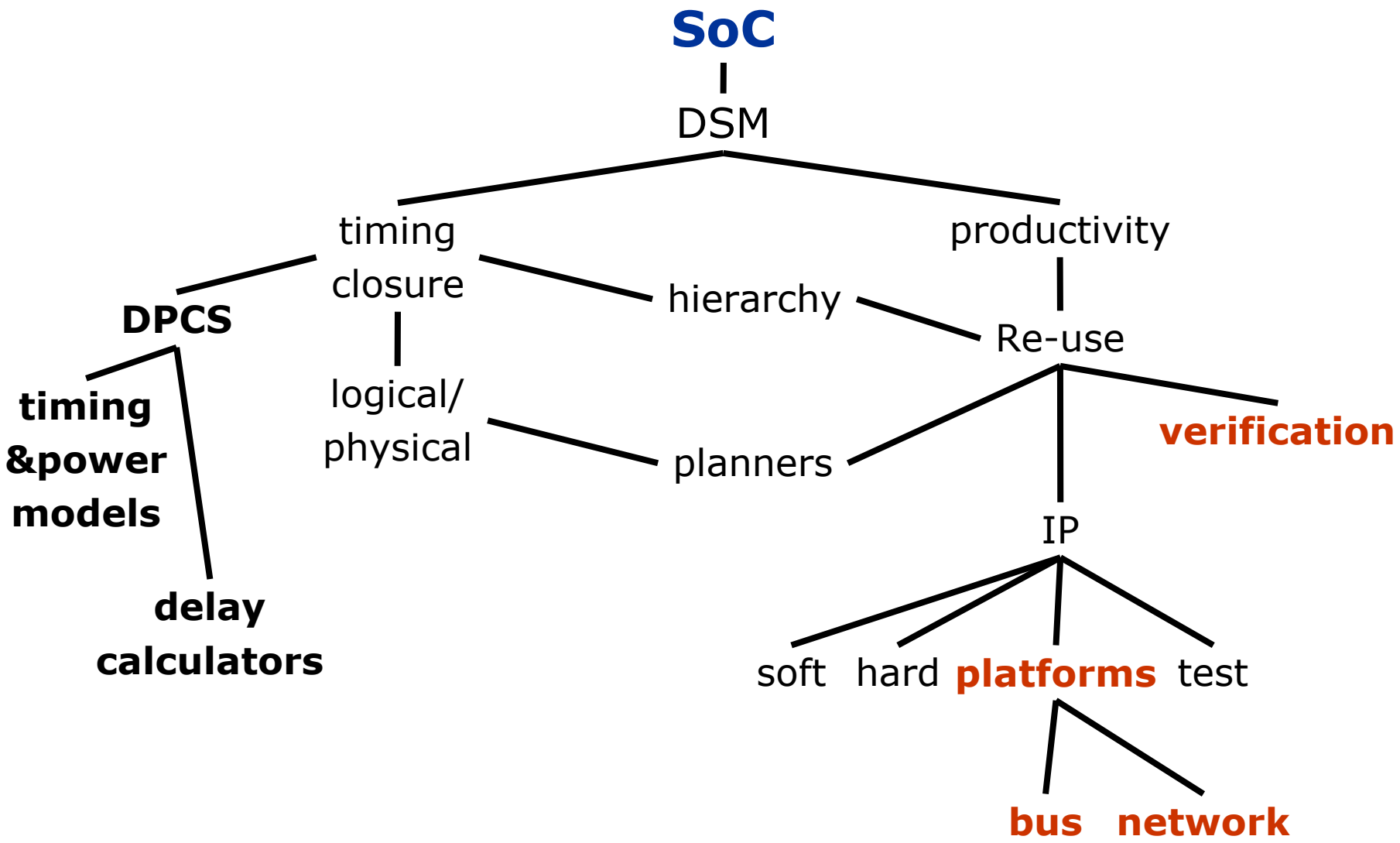

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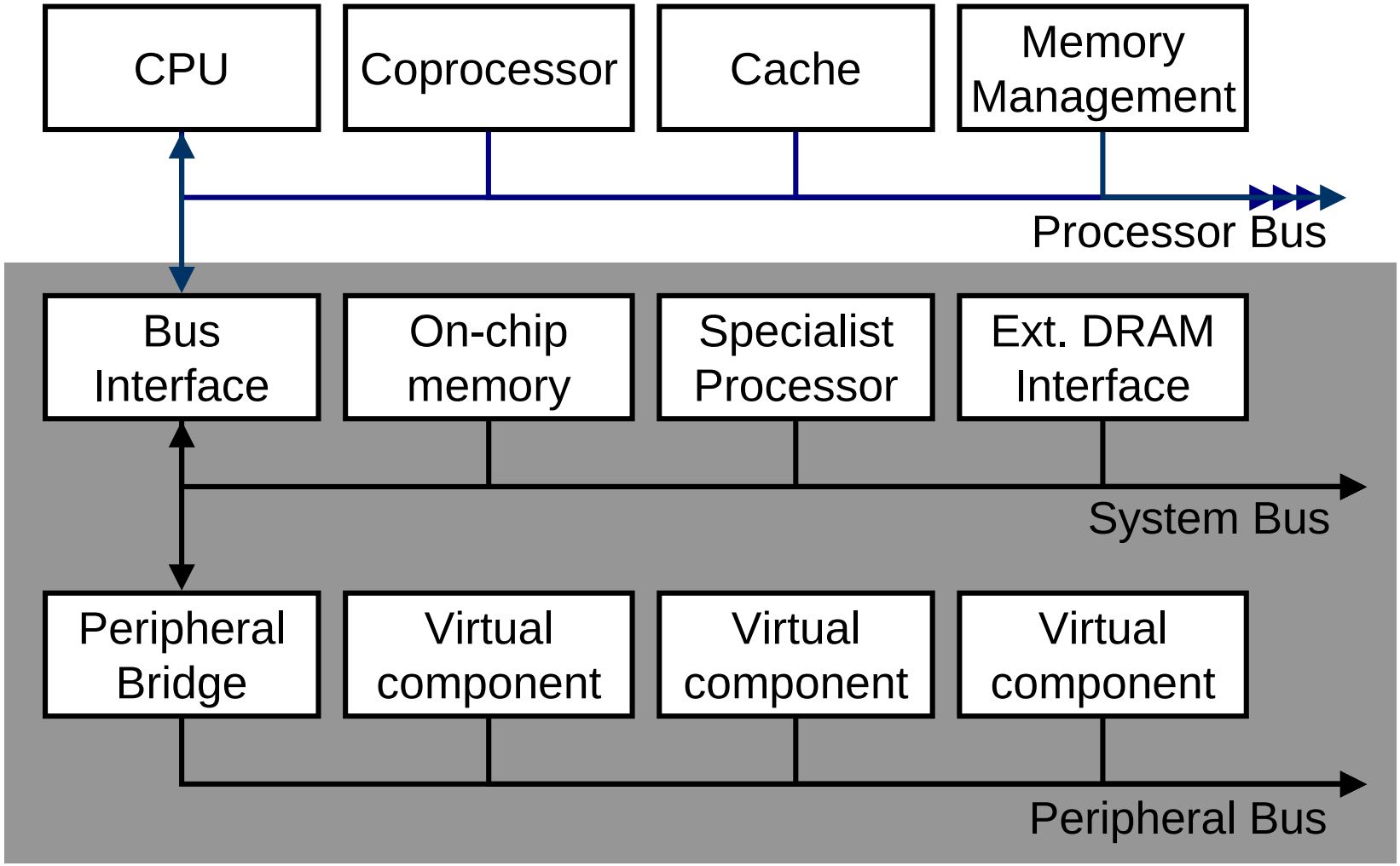
SoC generic platform architecture



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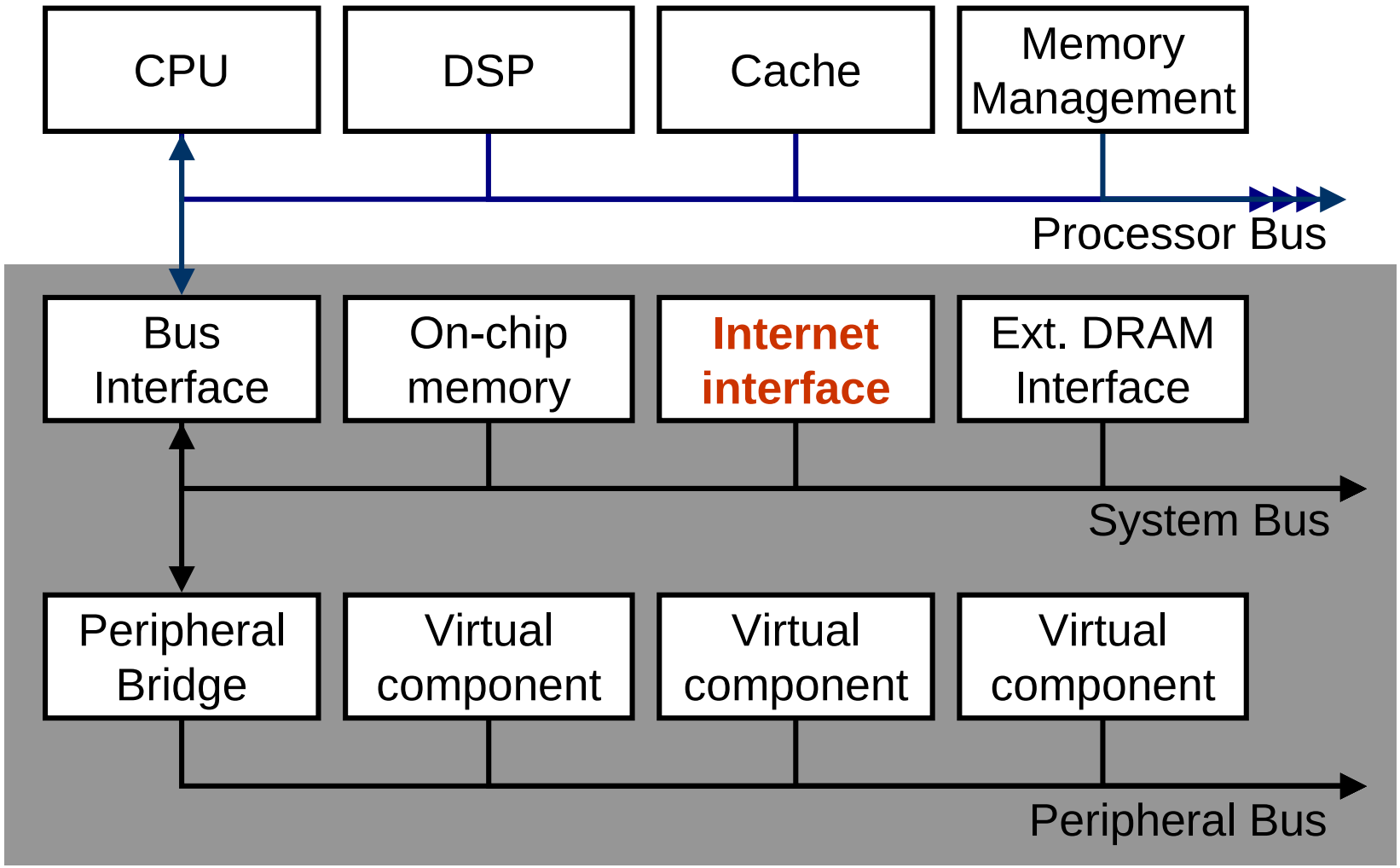
Internet information appliance



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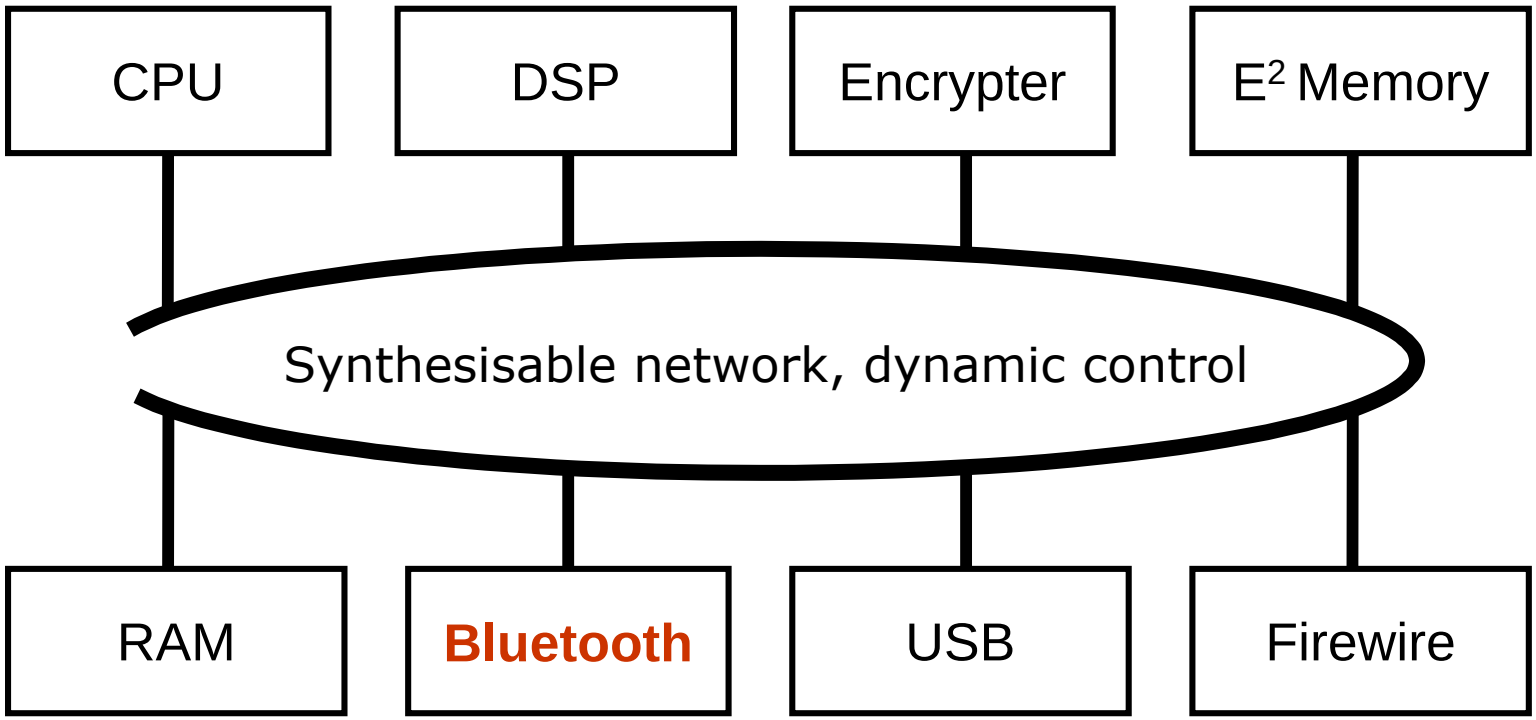
Network-based platform



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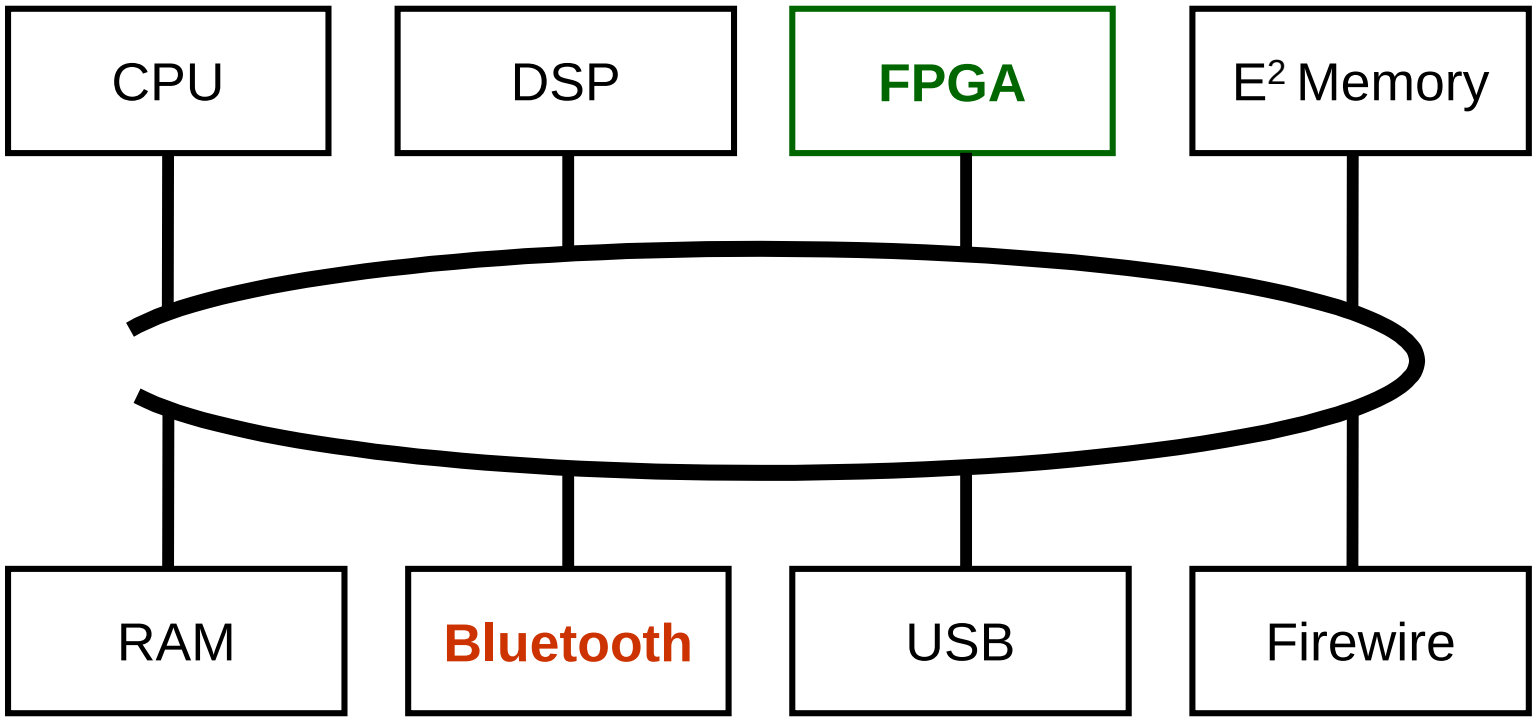
With FPGA for flexibility



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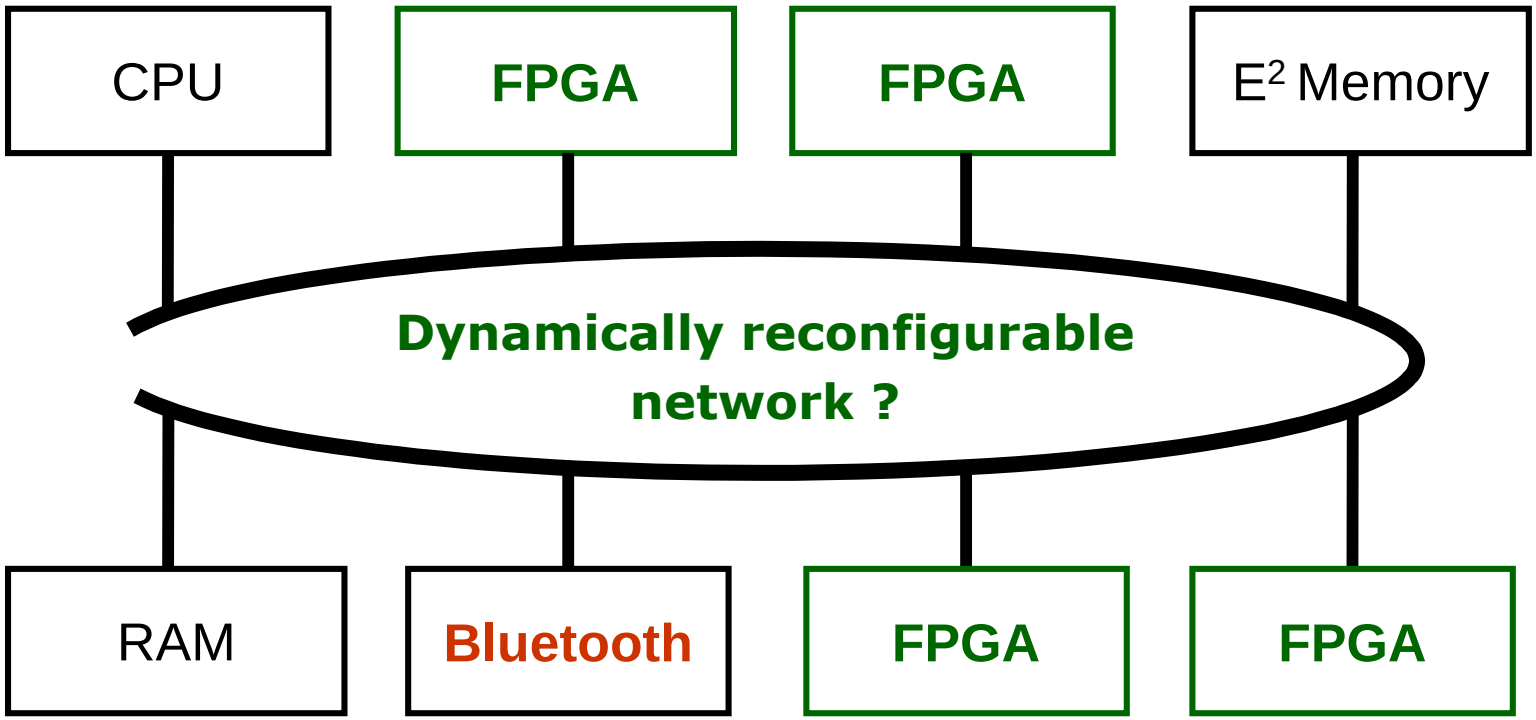
Or even, a dynamically architecture



Dynamically reconfigurable at the block level

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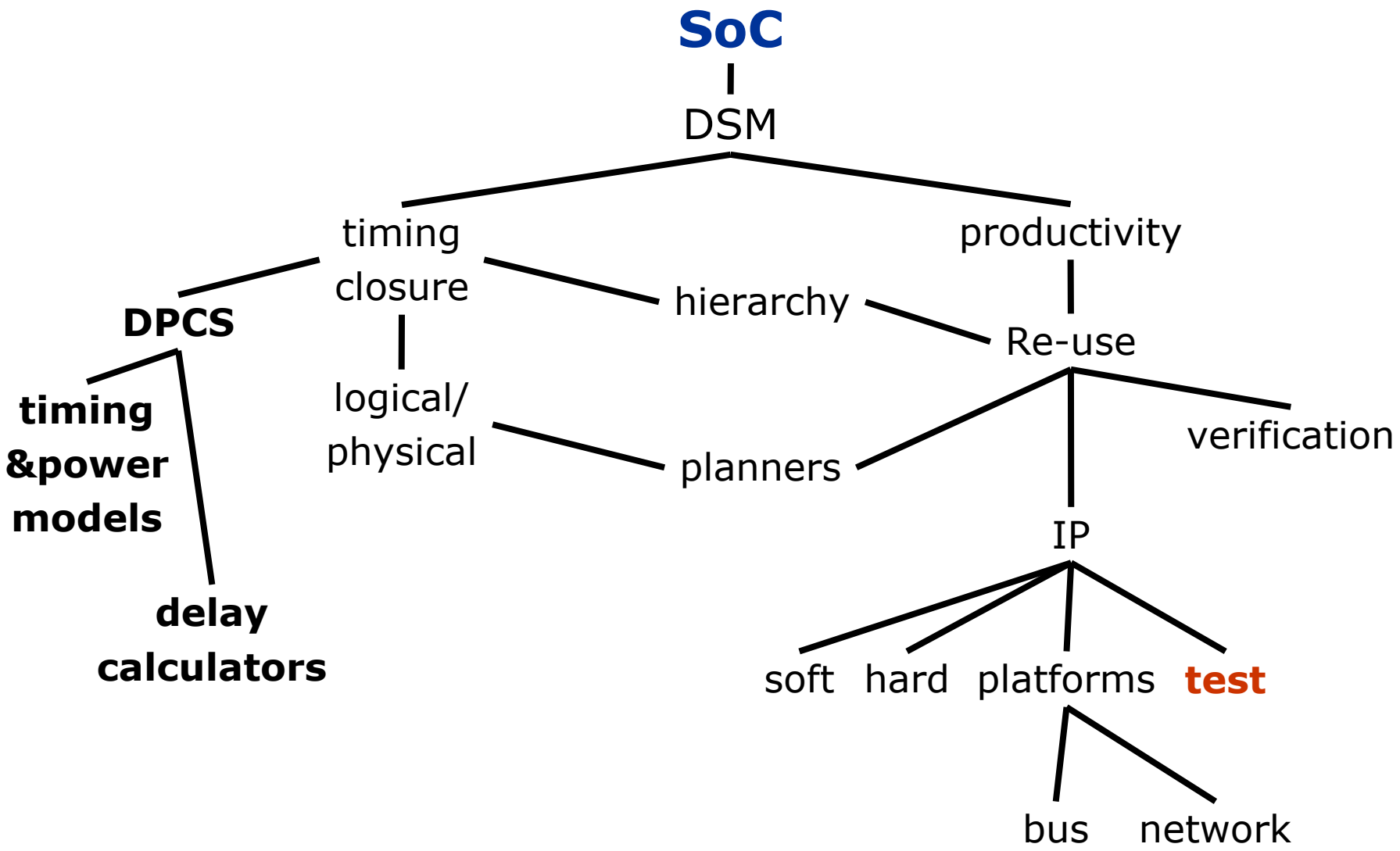

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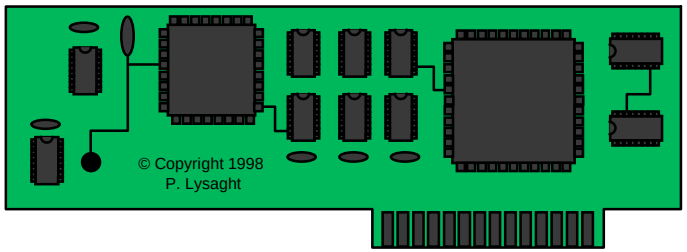
Large-scale design re-use is not new



Design re-use is the norm in PCBs. Re-use is typically very high

What is the problem in silicon?

PCBs have several critical advantages!

Components have all been tested and are known to be working before the board is loaded

All the components are accessible and can be replaced, if found to be faulty

Components are treated as true “black boxes” - not modified during the design process

SoRC is much simpler in these respects

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SoC test issues

- Integration of heterogeneous cores
- Expensive, multi-purpose ATE
- Core I/O ports may not be accessible from the SoC I/O pins
- Number of core I/O ports is not constrained by packaging
- More core I/O ports than SoC I/O pins means serial test access
- Bandwidth disparity between I/O pins and core logic

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Scan chains & boundary-scan for SoC?

- 1149.1 Boundary Scan is unsuitable for embedded core design
  - Serial test access => long test times
  - Access constraints
  - Built-in self-test (BIST) operations halt other tests
  - Does not natively support hierarchy

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IEEE P1500 Embedded Core Test Working Group

- Mission statement

  "Standardise the information model and test interface (access and control) between a non-mergeable core and its host (the system-on-chip or next level of core), in order to facilitate core TEST interoperability (plug-and-play) and hence improve the efficiency of core providers, users, and manufacturers."

- Proposals
  - Test Wrapper
  - Test Access Mechanism (TAM) not addressed

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P1500 Test Wrapper

- Functions required in embedded core test
  - Normal Operation (Wrapper is invisible)
  - Interconnect test
  - Isolation
  - Bypass
  - Control for switching wrapper modes
- Capabilities required at core I/O ports
  - I/O observation
  - I/O control
    - Test vector application and results capture
    - I/O constraint
    - Output disable

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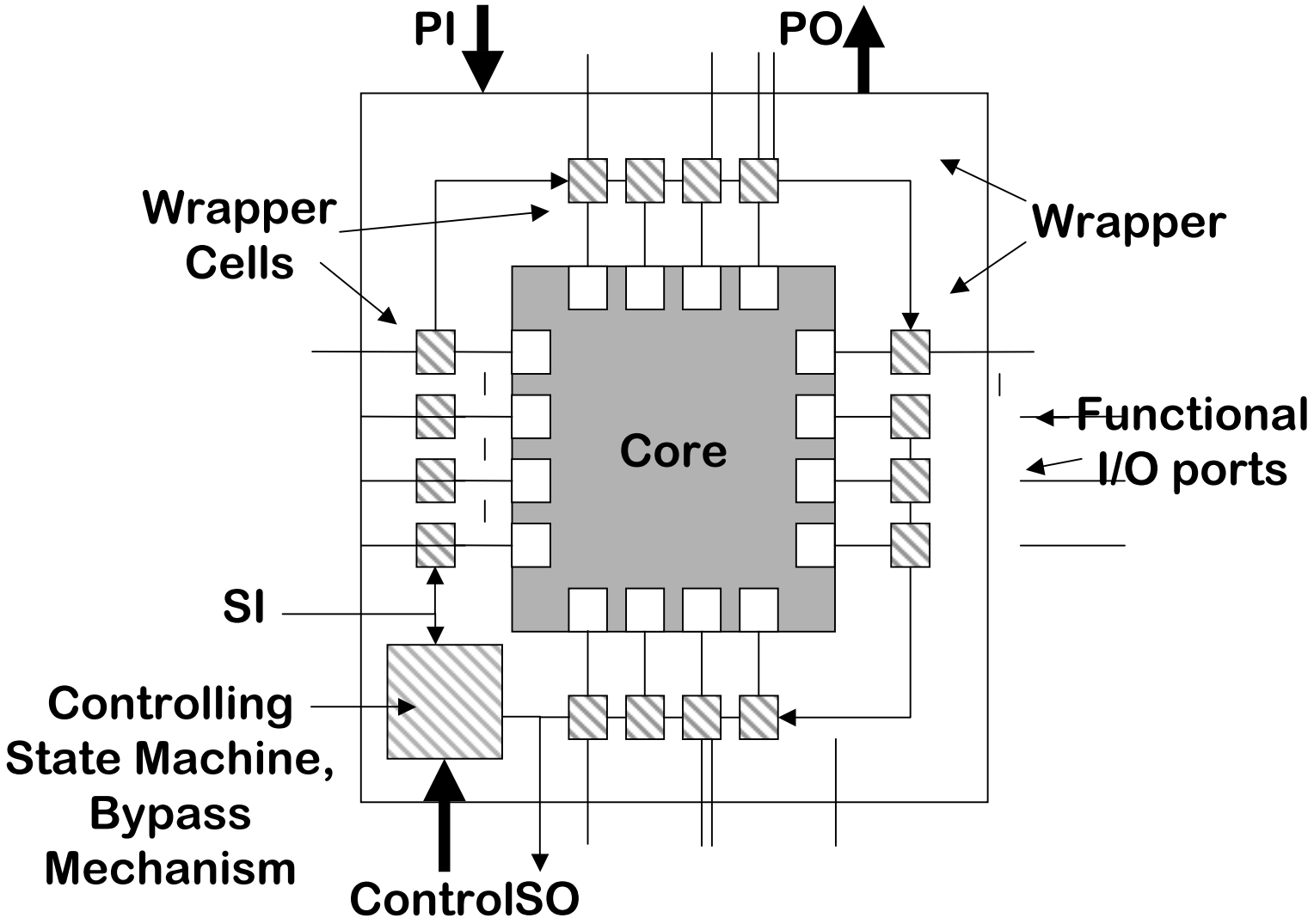
P1500 Test Wrapper



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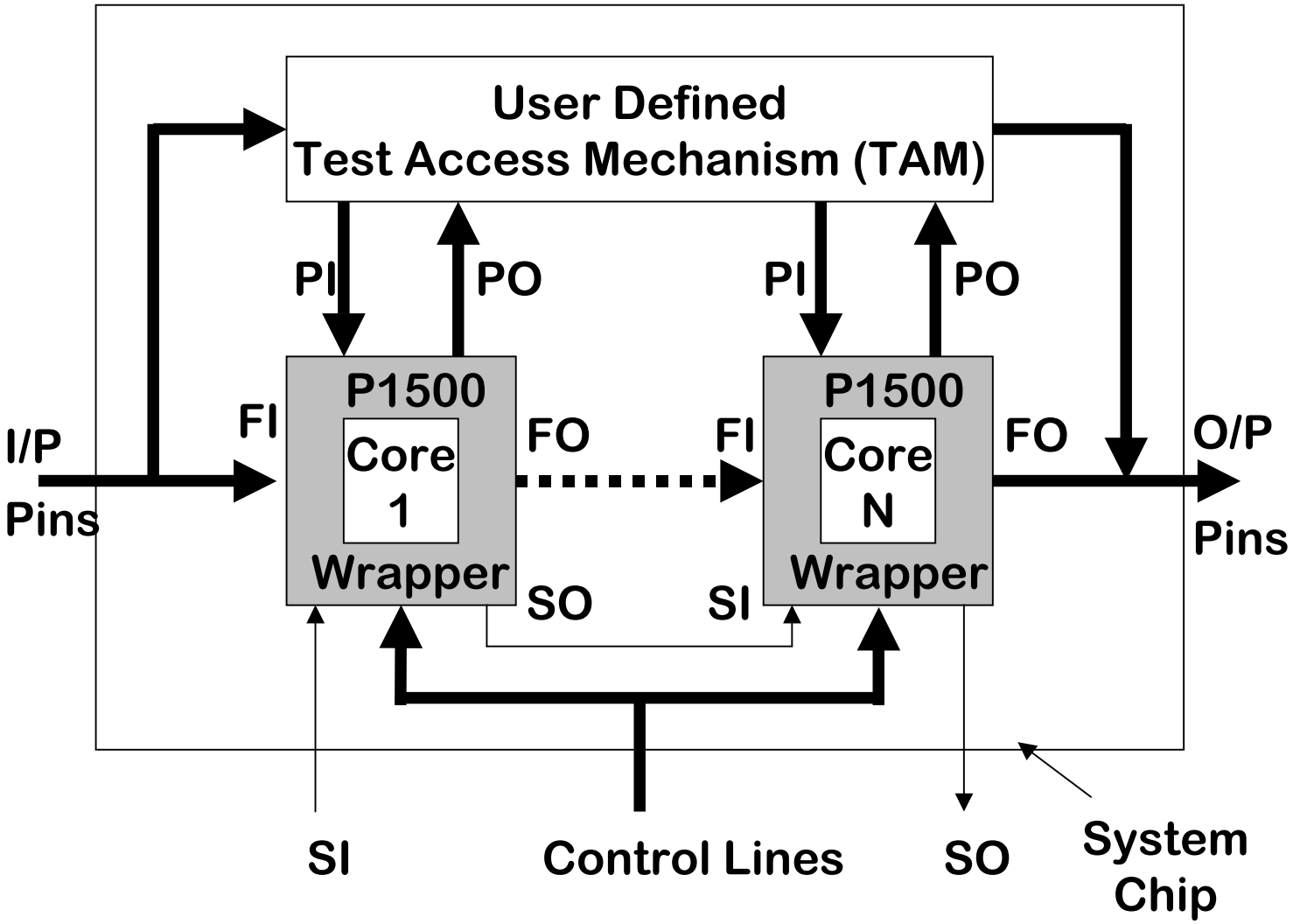
Use the FPGA core as the TAM?



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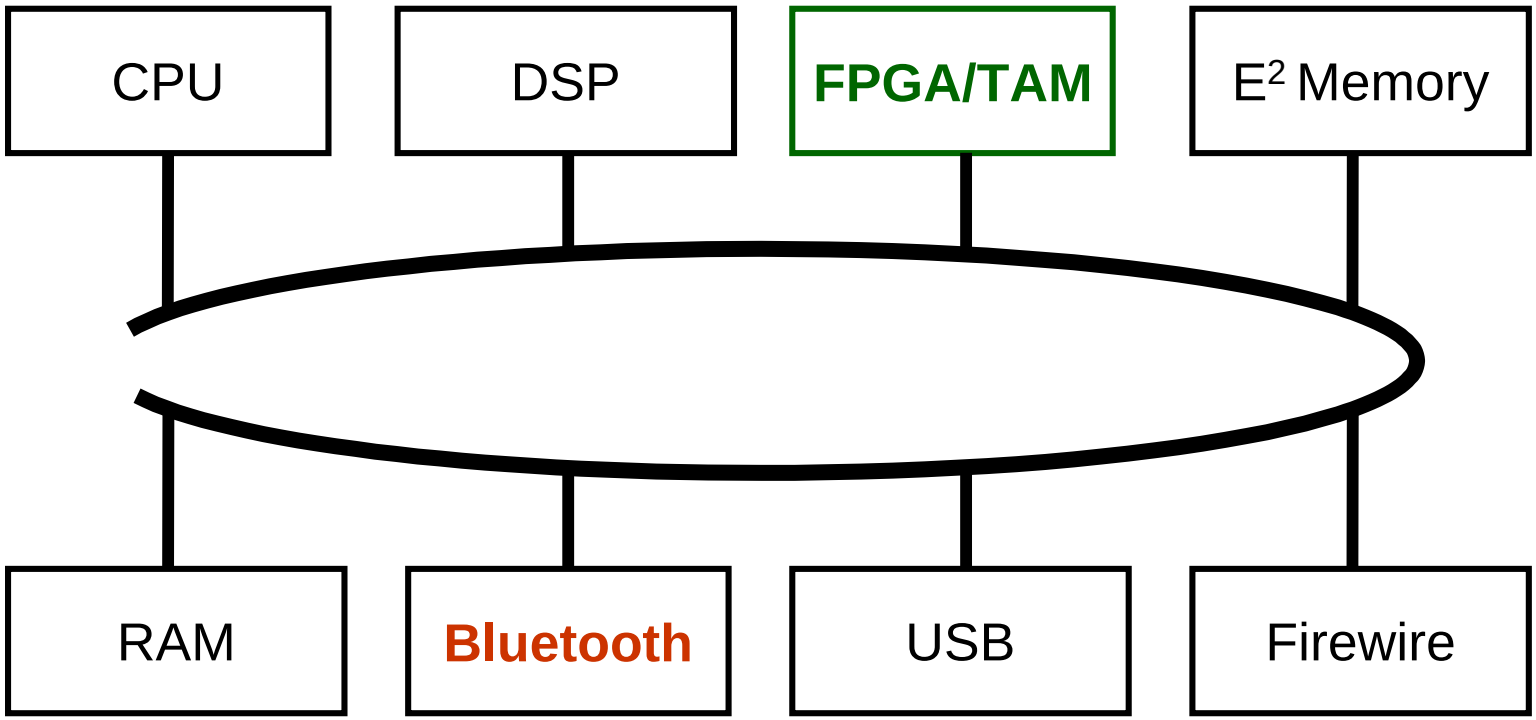
DR Test Access Method



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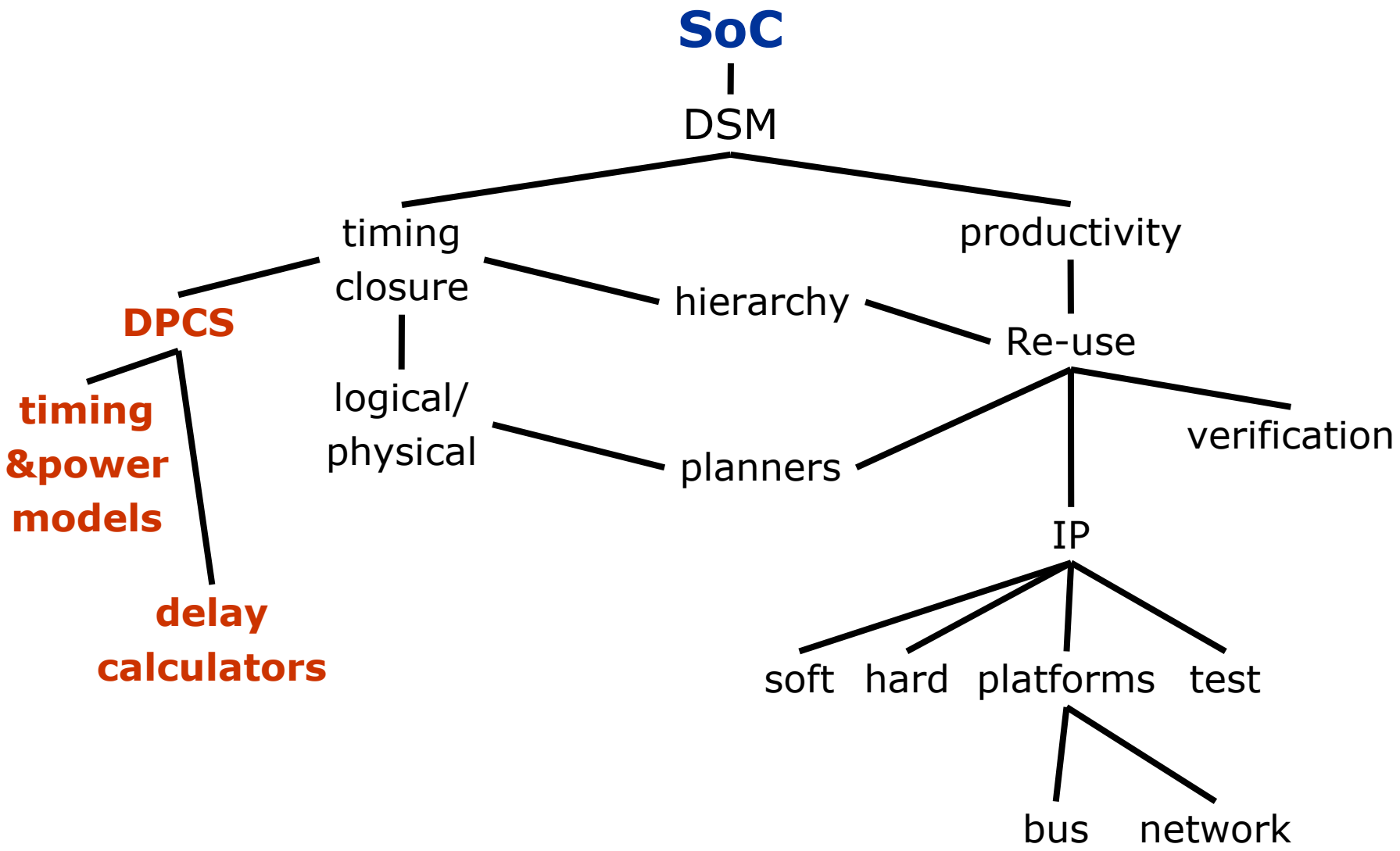

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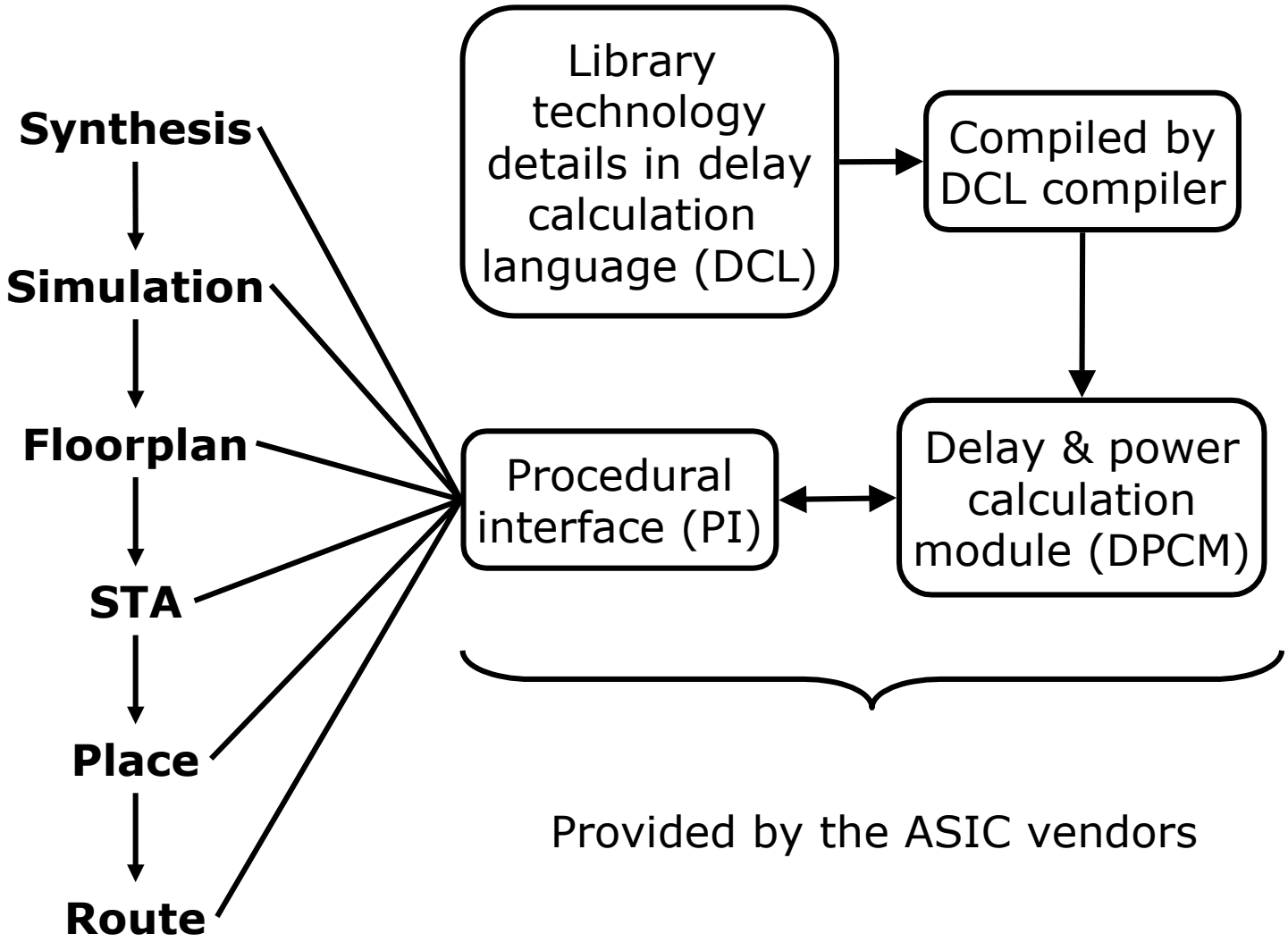
OLA/DCL



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DPCS

- Delay and power calculation system (DPCS)
  - Calculation and modeling of delay and power for DSM
- Delay calculation language (DCL)
  - Optimised for timing and power calculations
  - Flexible and extensible
  - Range of speed accuracy trade-offs in representing timing and power information (look-up tables, equations, etc)
- Delay and power calculation module (DPCM)
  - Dynamically linked library with procedure interface (PI) for communicating with CAD tools

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Benefits

- Genuine standard
  - OVI - SI2 - IEEE 1481
- Common interface for all design tools and stages
- Consistent results with different CAD tools
- Dynamically loaded, shared binary executable
- One interface for all ASIC and CAD tool vendors
- Protects IP in libraries (encryption and compilation - US legal requirement)
- Technology proven within IBM

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DRL?

- Hierarchical timing models?
- Don’t really know?

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Summary

- The high-end ASIC flow has changed dramatically
- Logical and physical design are integrated
- Hierarchy and structure are now important
- Re-use based on pre-verified IP is crucial
- SoC is achieving changes that DRL alone could not
- New possibilities in FPGA design, IP, platforms, test
- Re-use extends beyond tools and circuits to human knowledge

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Finally

- Marketing said …

1. Paperless office
(I should have bought shares in paper companies)

2. E-commerce, dot.com
(I should have bought shares in DHL & Fed Ex)

3. Reconfigurable computing
(I should have bought shares in ARM)

4. PC-less world
(I am beginning to wonder about that guy in marketing)

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